MPC5xx/8xx Debugger and Trace

TRACE32 Online Help

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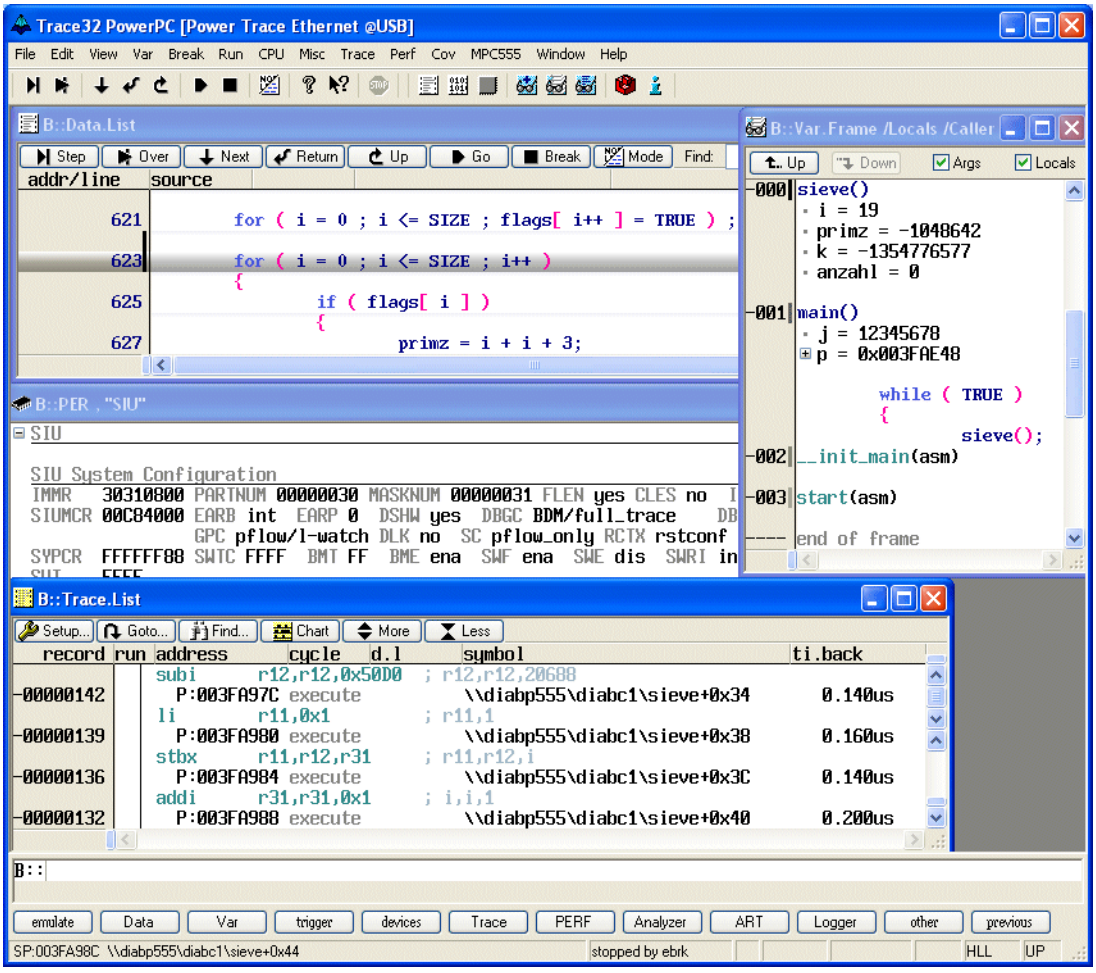
30-Jun-14 TrBus.Out and TrBus.Set were moved to general_ref_t.pdf.


Trace32 PowerPC [Power Trace Ethernet @USB]
File Edit View Var Break Run CPU Misc Trace Perf Cov MPC555 Window Help
B::Data.List
Step Over Next Return Up Go Break Mode Find:
addr/line source
621 for (i = 0 ; i <= SIZE ; flags[i++] = TRUE) ;
623 for (i = 0 ; i <= SIZE ; i++)
625 if (flags[i])
627 primz = i + i + 3;
B::Var.Frame /Locals /Caller
Up Down Args Locals
000 sieve()
i = 19
primz = -1048642
k = -1354776577
anzahl = 0
001 main()
j = 12345678
p = 0x003FAE48
while (TRUE)
sieve();
002 __init_main(asm)
003 start(asm)
---- end of frame
B::PER , "SIU"
SIU
SIU System Configuration
IMMR 30310800 PARTNUM 00000030 MASKNUM 00000031 FLEN yes CLES no
SIUMCR 00C84000 EARB int EARP 0 DSHW yes DBGC BDM/full_trace
GPC pflow/l-watch DLK no SC pflow_only RCTX rstconf
SYPCR FFFFFF88 SWTC FFFF BMT FF BME ena SWF ena SWE dis SWRI in
B::Trace.List
Setup... Goto... Find... Chart More Less
record run address cycle d.l symbol ti.back
-00000142 subi r12,r12,0x50D0 ; r12,r12,20688
P:003FA97C execute \\diabp555\diabc1\sieve+0x34 0.140us
li r11,0x1 ; r11,1
-00000139 P:003FA980 execute \\diabp555\diabc1\sieve+0x38 0.160us
stbx r11,r12,r31 ; r11,r12,i
-00000136 P:003FA984 execute \\diabp555\diabc1\sieve+0x3C 0.140us
addi r31,r31,0x1 ; i,i,1
-00000132 P:003FA988 execute \\diabp555\diabc1\sieve+0x40 0.200us
B::
emulate Data Var trigger devices Trace PERF Analyzer ART Logger other previous
SP:003FA98C \\diabp555\diabc1\sieve+0x44
stopped by ebrk
HLL UP

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Brief Overview of Documents for New Users

Architecture-independent information:

- **"Debugger Basics - Training"** (training_debugger.pdf): Get familiar with the basic features of a TRACE32 debugger.
- **"T32Start"** (app_t32start.pdf): T32Start assists you in starting TRACE32 PowerView instances for different configurations of the debugger. T32Start is only available for Windows.
- **"General Commands"** (general_ref_<x>.pdf): Alphabetic list of debug commands.

Architecture-specific information:

- **"Processor Architecture Manuals"**: These manuals describe commands that are specific for the processor architecture supported by your debug cable. To access the manual for your processor architecture, proceed as follows:

  - Choose **Help** menu > **Processor Architecture Manual**.

- **"RTOS Debugger"** (rtos_<x>.pdf): TRACE32 PowerView can be extended for operating system-aware debugging. The appropriate RTOS manual informs you how to enable the OS-aware debugging.

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NOTE:	To prevent debugger and target from damage it is recommended to connect or disconnect the debug cable only while the target power is OFF. Recommendation for the software start: 1. Disconnect the debug cable from the target while the target power is off. 2. Connect the host system, the TRACE32 hardware and the debug cable. 3. Power ON the TRACE32 hardware. 4. Start the TRACE32 software to load the debugger firmware. 5. Connect the debug cable to the target. 6. Switch the target power ON. 7. Configure your debugger e.g. via a start-up script. Power down: 1. Switch off the target power. 2. Disconnect the debug cable from the target. 3. Close the TRACE32 software. 4. Power OFF the TRACE32 hardware.

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Starting up the BDM Debugger is done by the following steps:

1. Select the device prompt B: for the TRACE32 ICD-Debugger, if the device prompt is not active after starting the TRACE32 software.

```
b:
```

2. Select the CPU type to load the CPU specific settings.

```
SYStem.CPU MPC563
```

The default CPU is the MPC860.

3. Inform the debugger where's FLASH/ROM on the target, this is necessary for the use of the on-chip breakpoints.

```
MAP.BOnchip 0x100000++0x0fffff
```

On-chip breakpoints are now used, if a program or spot breakpoint is set within the specified address range. A list of all available on-chip breakpoints for your architecture can be found under **On-chip Breakpoints**.

4. Enter debug mode.

```
SYStem.Up
```

This command resets the CPU, enables the debug mode and stops the CPU at the first opfetch (reset vector). After this command is possible to access memory and registers.

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5. Configure the IBUS.

```
SYStem.Option IBUS NONE      ; No show cycles are performed.
                             ; Recommended for BDM debugger only.

SYStem.Option IBUS IND       ; Show cycles are generated for all
                             ; indirect changes in the program flow.
                             ; Recommended if a RISC Trace or
                             ; PowerTrace module is connected.
```

Set the special function registers to prepare your target memory for program loading.

```
Data.Set SPR:027E %Long 0x800
```

6. Load the program.

```
Data.LOAD.Elf diabp555.x     ; Load ELF file
```

The load command depends on the file format generated by your compiler. For more information refer to **Compiler**. A full description of the **Data.Load** command is given in the **"General Commands Reference"**.

The start up sequence can be automated using the script language PRACTICE. A typical start sequence is shown below:

```
b::                              ; Select the ICD-Debugger device
                                 ; prompt

WinCLEAR                         ; Delete all windows

MAP.BOnchip 0x100000++0x0fffff   ; Specify where's FLASH/ROM

SYStem.CPU 0x563                 ; Select the processor type

SYStem.Up                        ; Reset the target and enter debug
                                 ; mode

Data.LOAD.Elf diabp563.x         ; Load the application

Register.Set PC main             ; Set the PC to the function main

Data.List                        ; Open a source listing *)

Register /SpotLight              ; Open the register window *)

Frame.view /Locals /Caller       ; Open the stack frame with
                                 ; local variables *)

Var.Watch %Spotlight flags ast   ; Open watch window for variables *)

PER.view                         ; Open a window for the special
                                 ; function registers
```

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```
Break.Set sieve                    ; Set breakpoint to function sieve

Break.Set 0x1000 /Program          ; Set a software breakpoint to address
                                   ; 1000 (address 1000 is in RAM)

Break.Set 0x101000 /Program        ; Set an on-chip breakpoint to address
                                   ; 101000 (address 101000 is in FLASH)
```

*) These commands open windows on the screen. The window position can be specified with the **WinPOS** command. Refer to the **PEDIT** command to write a script and to the **DO** command to start a script.

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General

- Locate the BDM connector as close as possible to the processor to minimize the capacitive influence of the line length and cross coupling of noise onto the BDM signals.

Ensure that the debugger signal ($\overline{\text{HRESET}}$) is connected directly to the $\overline{\text{HRESET}}$ of the processor. This will provide the ability for the debugger to drive and sense the status of $\overline{\text{HRESET}}$. The target design should only drive the HRESET with open collector, open drain. $\overline{\text{HRESET}}$ should not be tied to $\overline{\text{PORESET}}$, because the debugger drives the HRESET and DSCK to enable BDM operation.

- The TRACE32 internal buffer/level shifter will be supplied via the VCCS pin. Therefore it is necessary to reduce the VCCS pull-up on the target board to a value smaller 10 Ω.

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RESET Configuration

At HRESET the Hard Reset Configuration bits will be sampled. Depending on the $\overline{\text{RSTCONF}}$ pin the external or the internal configuration word is sampled.

RSTCONF	Configuration Word
0	DATA[0..31] pins
1	internal data default word (0x0000 0000)

The multifunction I/O pins (VFLS0/1) have to be configured correctly for the debugging. Drive actively the following pins:

MPC5xx DBGC(D9,D10) and DBPC(D11)

MPC8xx DBGC(D9,D10) and DBPC(D11,D12)

There are two signal schemes possible to indicate the processor status to the debugger. Option A is recommended but Option B is also supported for the BDM functionality.
Option B is used as an alternative to eliminate pin conflicts. Option B is typically used if:

- the internal watchpoints are used
- the amount of signals must be reduced to a minimum
- the target design uses PCMCIA Port B.

Option A: Using the VFLS pins

MPC800: (DBGC=[11]; DBPC=0; FRC=x)
MPC500: (DBGC=[00,10]; DBPC=0; GPC=x)

Comment	Signal Name	PIN	PIN	Signal Name	Comment
	IPB0/IWP0/VFLS0	1	2	/SRESET	
	GND	3	4	DSCK/TCK	
	GND	5	6	IP_BI/IWP1/VFLS1	
	HRESET	7	8	DSDI/TDI	
	VCCS	9	10	DSDO/TDO	

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Option B: Using the FREEZE pin

MPC800: (DBGC=[11]; DBPC=0; FRC=0)
MPC500: (DBGC=[00,10]; DBPC=0; GPC=[10,11])

Comment	Signal Name	PIN	PIN	Signal Name	Comment
	FRZ/IRQ6	1	2	/SRESET	
	GND	3	4	DSCK/TCK	
	GND	5	6	FRZ/IRQ6	
	HRESET	7	8	DSDI/TDI	
	VCCS	9	10	DSDO/TDO	

If option B is used, the **SYStem.Option.FreezePin** must be switched on

When the PowerPC's development port (BDM) is used, the JTAG functionality is disabled.

BDM Termination

T32 PU/ PD	Target PU/PD	Signal Name	PIN	PIN	Signal Name	Target PU/PD	T32 PU/PD
-	47kPU	FRZ/ VFLS0	1	2	/SRESET	10kPU	-
-	-	GND	3	4	DSCK	10kPD	4k7PD
-	-	GND	5	6	FRZ/ VFLS1	47kPU	-
10kPU	10kPU	HRESET	7	8	DSDI	10kPD	4k7PD
-	<10	VCCS	9	10	DSDO	>10k	-

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The CPU handles the debug mode similar to an exception.

SYStem.Option BRKNOMSK OFF: The program execution is not stopped as long as the processor is in a non-recoverable state (RI bit cleared in the Machine Status register).

SYStem.Option BRKNOMSK ON: The program execution can be stopped by a breakpoint even if the processor is in a non-recoverable state. Since the debug exception overwrites SRR0 and SRR1 it is not advisable to continue the debugging process.

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SYStem.Up Errors

The **SYStem.Up** command is the first command of a debug session where communication with the target is required. If you receive error messages while executing this command this may have the following reasons:

- The target has no power.
- The pull-up resistor between the JTAG/COP[VCCS] pin and the target VCC is too large.
- The target is in reset: The debugger controls the processor reset and use the RESET line to reset the CPU on every SYStem.Up.
- There is logic added to the JTAG/COP state machine: The debugger supports only one processor on one JTAG chain. Only the debugged processor has to be between TDI and TDO in the scan chain. No further devices or processors are allowed.
- There are additional loads or capacities on the JTAG lines.

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Debugging via VPN	**The debugger is accessed via Internet/VPN and the performance is very slow. What can be done to improve debug performance?** The main cause for bad debug performance via Internet or VPN are low data throughput and high latency. The ways to improve performance by the debugger are limited: in practice scripts, use "SCREEN.OFF" at the beginning of the script and "SCREEN.ON" at the end. "SCREEN.OFF" will turn off screen updates. Please note that if your program stops (e.g. on error) without executing "SCREEN.OFF", some windows will not be updated. "SYStem.POLLING SLOW" will set a lower frequency for target state checks (e.g. power, reset, jtag state). It will take longer for the debugger to recognize that the core stopped on a breakpoint. "SETUP.URATE 1.s" will set the default update frequency of Data.List/ Data.dump/Variable windows to 1 second (the slowest possible setting). prevent unneeded memory accesses using "MAP.UPDATEONCE [address-range]" for RAM and "MAP.CONST [address--range]" for ROM/ FLASH. Address ranged with "MAP.UPDATEONCE" will read the specified address range only once after the core stopped at a breakpoint or manual break. "MAP.CONST" will read the specified address range only once per SYStem.Mode command (e.g. SYStem.Up).

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Setting a Software Breakpoint fails	**What can be the reasons why setting a software breakpoint fails?** Setting a software breakpoint can fail when the target HW is not able to implement the wanted breakpoint. Possible reasons: The wanted breakpoint needs special features that are only possible to realize by the trigger unit inside the controller. Example: Read, write and access (Read/Write) breakpoints ("type" in Break.Set window). Breakpoints with checking in real-time for data-values ("Data"). Breakpoints with special features ("action") like TriggerTrace, TraceEnable, TraceOn/TraceOFF. TRACE32 can not change the memory. Example: ROM and Flash when no preparation with FLASH.Create, FLASH.TARGET and FLASH.AUTO was made. All type of memory if the memory device is missing the necessary control signals like WriteEnable or settings of registers and SpecialFunctionRegisters (SFR). Contrary settings in TRACE32. Like: MAP.BOnchip for this memory range. Break.SELect.<breakpoint-type> Onchip (HARD is only available for ICE and FIRE). RTOS and MMU: If the memory can be changed by Data.Set but the breakpoint doesn't work it might be a problem of using an MMU on target when setting the breakpoint to a symbolic address that is different than the writable and intended memory location.
Sporadic Debug Port Fail	**The debugger crashes sporadically when a dump window is open or a system up is sometimes not possible.** Be sure that the "VCC PIN" of the debug port connector is connected directly to the VCC of your target board. The Lauterbach debugger uses this voltage to supply a buffer that drives the debug lines to the CPU. If there is a resistor between the VCC of your board and our VCC pin, our supply voltage might drop too low.
MPC5XX/8XX Cannot write to SYPCR	**Writing SYPCR has no effect.** The SYPCR register can only be written one time. If the SYSTEM.OPTION.WATCHDOG is set to OFF then the CPU WATCHDOG function will be disabled by the debugger during a SYSTEM.UP. To disable the WATCHDOG on the CPU the debugger writes to SYPCR and uses the one-time write access to the SYPCR register.

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MPC5XX/8XX ICTRL register access	**Write access to the ICTRL register by the program does not take any effekt!** If BDM (background debug mode) is enabled, the ICTRL register CAN NOT be modified through the program and can only be modified through RCPU development access (by debugger). [MPC565 user manual, chapter 23.2.5.1 Program Trace Guidelines] The BDM is enalbed if the Debugger is connected and CPU is up. (e.g. SYStem.Mode.Up, SYStem.Mode.Go) The BDM is disabled even if the debugger is connected when SYStem.Mode.NoDebug is used. The debug mode will be enable with a DSCK assert HIGH while SRESET asserted. SRESET _____/---------- DSCK ----------xxxxxxxxxxxx If there is no debugger connected and there is the same behavior, maybe a pull-up at DSCK causes the BDM automatically. Note: Use the SYStem.Option.IBUS [xxx] to set the ICTRL[ISCT_SER] bits. Manual access to the ICTRL register (SPR 158./0x9E) will be overwritten by the debugger with each Step or Go!
MPC5XX/8XX Step or Go can't be executed Successful	**Step or go result in a error message!** ... VFLS0/1 pins have wrong status. Freeze connected? sys.o.freeze VFLS from MIOS modul used? PU is missing 10 kOhm Right after reset VFLS pins are also inputs! State is non-recoverable!

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MPC5XX/8XX With connected debugger program behaves in a different way	**With connected debugger program behaves in a different way** sys.o.ibus == debug register ibus has priority, register will be overwritten. RSTCONF for IBUS will be overwritten. sys.nodebug only will not enable the BDM interface. sys.o.freeze.off (default) assumes VFLS0/1 at BDM connector and overwrites SIUMCR bits. (MPC8XX)
MPC8XX/5XX Exceptions and Stepping	**What happens if I debug my code and an exception occurs?** The MPC8xx/5xx can react in two ways when an exception occurs: The exception is handled by the exception handler. This way the exception is not detected by the debugger (default). The program execution is stopped at the exception and the debug mode is entered, if the exception is enabled by the command "TrOnchip.Set <exception>". Refer also to the description of the Debug Enable Register in your processor manual. TRACE32 displays the reason for the program stop in the state line (refer also to the Exception Cause Register description in your processor manual). The program execution is stopped in most cases exactly at the instruction that caused the exception, in some cases at the next instruction. On some exceptions it is not possible to continue the debugging.

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MPC8XX/5XX Software runs differently with ICD	**The target runs fine without the ICD attached. But with the ICD attached, the target runs for a while and then it hangs up.** If the debug mode is enabled, the serialize control bit and the instruction fetch show cycle control bits are set to SERALL after reset. In SERALL mode the processor is fetch serialized and all internal fetch cycles appear on the external bus. The processor performance is, therefore, much slower. If only a BDM debugger is used perform the command "SYStem.Option IBUS NONE". In NONE mode the processor works in normal mode and no show cycles are performed. There is no performance degradation in this mode. If a RISC Trace or a PowerTrace is used, perform the command "SYStem.Option IBUS IND". In IND mode the processor works in normal mode and show cycles are performed for all indirect changes in the program flow. The performance degradation in this mode is about 1 %. For more information refer to the description of the ISCT_SER register in your processor manual.
MPC8XX/5XX Using NOTRAP Option	**How do I use the TRAP exeption for my own application?** Use the command SYStem.Option NOTRAP ON With this setting the TRAP exception is no longer used for software breakpoints. UNDEF 0 is used instead. Use the command TrOnchip.Set PRIE OFF With this setting the debug mode is no longer entered when a TRAP occurs. See also the Debug Enable Register in you processor manual. Now your application can handle the TRAP instruction.

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MPC8XX/5XX What means "stopped by SEI"?	**Where can I find more information about the acronyms SEIE, PRIE, MCIE, ...?** These names reflect the bits of the DER Register (Debug Enable Register), ECR (Exception Cause Register for MPC5xx family) and ICR (Interrupt Cause Register for MPC8xx family). The TRACE32 Debugger evaluate these bits all the time the processor change from running mode to stop status. The abbreviation of these corresponding exceptions/interrups handler differ a little bit between the MPC5xx and MPC8xx family and several sub-derivatives manual. Additional Information: In a debug session almost all exception could be used/enabled/configured to stop the CPU and enter the debug mode instead of executing the corresponding exception handler. This could be set up in the T32 PowerView Menue: Break - OnChip_Trigger - Set - [MCIE] (MCIE is used as example here) or alternatively in the command line or script language: TrOnchip.Set [MCIE] ON If the option is enabled (box is checked), the CPU will stop right at the instruction cause this exception/interrupt and enter the debug mode.
MPCXXX Runtime Accuracy	**When stepping with the ICD debugger, the runtime counter shows too long count values.** The runtime counter unit of the PowerPC debugger is realized using a software counter of the host and a hardware counter of the Lauterbach tool. The accuracy is about 10 us.
MPCXXX Verify Error at Single-Step or Breakpoint	**I get the error message: verify error at address ...,** By default TRACE32-ICD uses software breakpoints to set a breakpoint to an instruction. Software breakpoint means the original instruction is replaced by to TRAP in order to stop the program. This is the reason why a software breakpoint usually requires that the instruction is in RAM. Otherwise the error message verfiy error at address (address) is displayed. The reasons for these errors are: The instruction is in ROM/FLASH/EPROM. To set software breakpoints in FLASH refer to the command "FLASH.Auto". The appropriate CS is switched to ReadOnly mode. In this case it is not possible to patch the code. It is possible to use a limited number of on-chip breakpoints to set a breakpoint to ROM/FLASH/EEPROM or ReadOnly memories. For more information refer to the command "MAP.BOnchip <range>".

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Connect a Nexus Probe to a PowerTrace Unit	**How do I correctly connect a Nexus Probe to a PowerTrace unit?** A Nexus probe has one, two or three ribbon cables for the connection to the PowerTrace unit. The PowerTrace has three connectors which are marked with A, B and C. (C is close to the black heatsink) Nexus probe connectors of newer probes are also marked with A, B and C. Place the appropriate cable into the corresponding connector. For older probes note the following: Probes with a single cable: connect the ribbon cable to connector C. Probes with two cables: connect the upper cable to connecter C, the second cable underneath to B. Probes with three cables: connect the upper cable to connecter C, the second cable underneath to B and the third cable below to connector A. One does not require an additional JTAG dongle!
Incorrect Nexus-POD CPLD Revision	**What is the reason for "Incorrect Nexus-POD CPLD revision" message?** There are several reasons for the following message: Incorrect Nexus-POD CPLD revision - Please call technical support (refer to AREA) A wrong T32xxx.EXE has been executed (e.g. Super10.exe for a Copper-head probe) Just use the right SW. The current SW contains a new image for the CPLD on the probe. This reason is very seldom, but it may happen. One have to consider, that it is just a warning and normally one can continue using the debugger. However only for the case, the Area window shows a similar "expected CPLD revision number". It is recommended to contact your next support office. One will get a SW-Tool and some instructions how to fix it. The probe is defective. This reason can be recognized if the expected CPLD revision number is totally different from the current CPLD revision number, or even 0x00000 or 0xFFFFF. It is a serious reason and requires to send the probe back for repair. Also contact your local support office first.

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Missing Address Information on Top of the Trace	**Is there any reason why symbol addresses and names are not displayed from the beginning of the trace?** The Nexus protocol defines that a full address is transferred only occasionally, just in a Branch-Trace-Sync-Message and Data-Trace-Sync-Message. Most of the time only the significant portion of the current address is generated in the device and transferred in a Nexus message. Therefore the address can only be reconstructed and displayed after occurrence of a Sync-Message in the trace memory. A Sync messages is generated automatically after 255 messages latest. A single Nexus message without knowing what had happened before is useless! Look at the T.L /NEXUS , then one will see the location of the DTSM . After that location the address information is visible. A Sync message could be missing on top of the trace in the following cases: Any time Program is running before trace is in ARM state! Normally if analyzer is armed manually! In FIFO mode if trace memory overflows. Selective trace using Watchpoints Selective trace using CTU Some other cases.
Nexus Connector Pinout on Target	**I don't know exactly which signals from MCU must be connected to which** **signal on the AUX-port connector.** **Must certain signals be crossed ?** Not at all. The pin out one can find in the manual and at our home page, fits the description of Nexus standard from the target point of view. With other words, you have to connect the signals from the device to the appropriate signals with the same name on the connector. You must not take care about signal crossing.

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No or wrong Data in Nexus Trace

There are no or wrong Nexus Trace entries. What can be wrong ?

There are different reasons for the case the Nexus trace remains empty or the contents of the trace memory is not correct. Often this happens, if new prototype targets are used. Provided the Nexus probe is not defective, the Nexus probe - target connection should be investigated.

To prevent wrong trace analyzer settings by scripts, enter the command Analyzer.Reset and disable Performance Analysis , before checking the steps below.

First check if the Nexus probe or the extension cable is properly connected to the target.

To be able to trace Nexus messages, the appropriate trace signals must be activated, available at the connector

and they must fit timing and electrical demands.

Activation of trace signals is the job of the Trace32 SW. The user must not take care about.

The designer of the target is responsible for the availability of all relevant Nexus signals, according

to the Nexus standard specifications and the information one can find at the Lauterbach home page

(Adaptions/Connectors).

It is recommended to check the scheme of the target in case of problems.

The following trace signals (trace clock and status signals) are essential for trace capture:

MCKO, MSEO0 (and MSEO1 in case it is provided by the CPU). It is recommended to observe these

signals during real time program execution if the trace record counter does not change, despite the Analyzer

state is in ARM state. All two (three) signals must change their levels.

Trace data signals (MDO0 ... MDO15 , number depending on the aux port width) have to follow the same requirements

as the trace clock and control signals, but they can not prevent trace entries. They just can cause wrong trace entries.

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Electrical characteristics are normally given by the device on the target

Target Aux Port Connector Location and Extension Cables	**Can I use a longer extension cable?** Often customer ignore the warnings regarding the locaction of the aux port connector and regarding additional extension cables between the debugger and the target. This can cause a lot of trouble, especially for high speed applications. We strongly recommend to place the aux port connector as close as possible nearby the CPU. As closer as better. Take care about the signal trace length. Do not connect aux port signals to other connectors than the aux port connector and prevent signal stubs. Connect a proper termination to the signals coming from the probe, close to the CPU. Signals from the CPU to the probe should not be terminated. One can add 0 Ohm resistors in line of each Nexus signal close to the CPU. If necessary 0 Ohm can be replaced by a better value. The debugger does normally not need any pull-up or pull-down, except for reset. Care must just be taken just for non-Nexus signals. Bear in mind that the target needs possibly a pull-up or pull-down for certain signals if the debugger is not connected. Pay attention about the recommendations of the device manufacturer regarding the circuitry around the Nexus Aux port. We also recommend to use no other extension cables than the cables which come with the debugger. If possible do not use additional cables at all. Longer cables may work, but must not. It is the customers risk to use longer once as recommended. We can not guarantee proper operation.
MPC5XX/8XX Cannot write to SYPCR	**Writing SYPCR has no effect.** The SYPCR register can only be written one time. If the SYSTEM.OPTION.WATCHDOG is set to OFF then the CPU WATCHDOG function will be disabled by the debugger during a SYSTEM.UP. To disable the WATCHDOG on the CPU the debugger writes to SYPCR and uses the one-time write access to the SYPCR register.

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NEXUS-MPC56X Available Nexus Adaptions	**Which kind of Nexus adaptions are available for PowerPC debugging? Are converters also available?** Current Connections and Converters: **Preprocessor — to — Target — Order Nummer** **AMP40 (LA-7781) to AMP50 (LA-7786)** **to Glenair51 follows** **AMP50 (LA-7783) to AMP40 (LA-7784)** **to Glenair51 follows** **Glenair51 (LA-7782) to AMP40 (LA-7784)** **to AMP50 follows** **AMP40 8bit/MDO to AMP40 2bit/MDO (LA-7787)** **AMP50 8bit/MDO to AMP50 2bit/MDO (LA-7785)** If you need a different adaption it will take a few weeks to develop it. Some NEXUS connectors are shown in the file below. http://www.lauterbach.com/faq/nexcon.pdf Nexus Connectors
NEXUS-MPC56X AXIOM EVA-Board for 561/3	**If I change the CPU to MPC561/3 at the Axiom EVB, I have some problems to start the debugger on certain frequencies. What can I do?** It seems that the MPC561 and MPC563 is very sensitive about spikes, overshots and missing or wrong termination on the MCKI line. Unfortunately the current Axiom EVB has a very long open line at the base board to one of the Mictor connectors. To improve that behavior, cut the line DSCK/MCKI(J4-66) or/ and short cut the pins 3 - 4 at the BDM-Port connector by a jumper. For new target designs take care that the location of the NEXUS/READI connector is very close to the MCP561/3, the aux. port lines are as short as possible and terminate the lines correctly.

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NEXUS-MPC56X BDM-Debugport Fails after Changing Clock Frequency	**Why do I get a "emulator debug port problem" when I try to change the system clock via the System Clock SFRs?** (Taken from CUSTOMER ERRATA AND INFORMATION SHEET CDR_AR_924) READI: Communication is lost when clock freq. is changed while in BDM mode. ****** DESCRIPTION: When the READI is being used for BDM, a deadlock occurs when the development tool tries to enter a low-power mode or change the clock frequency (via the debug port). The internal clock will still run at the previous frequency. If code running on the target is changing the frequency then the following will occur: All READI MDI/MSEItraffic is ignored when this change is recognized. All MDO messages in the transmit FIFO will be sent. Then the MCKO will be stopped until the PLL has relocked at the new frequency. ****** WORKAROUND: Do not change the System Clock by the NEXUS debugger. Use the code running on the target to change the clock speed. Reset the READI module by asserting sreset_b or hreset_b to continue debugging after unsuccessfully changing the system frequency. ****** NOTE: In newer silicons this problem is fixed.
NEXUS-MPC56X Comparision PowerTrace-NEXUS to RISC Trace	**What is the difference between a Nexus Debugger and a BDM/RISC Trace configuration?** The main differences are listed in the document below. http://www.lauterbach.com/faq/nexus_vs_icr.pdf Differences

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NEXUS-MPC56X Debugger access during PLL setup	**What's the reason for "emulation debug port fail" during step over PLL setup ?** During PLL setup instructions it may happen that MCKO and MCKI are turned off for a certain time by the device. It depends on the PLL filter how long it lasts. Both clocks are important for the communication between the debugger and the device. If there is a communication request or a data transfer in progress during the missing clocks, it may happen that communication fails. A "Debug port fail" is the result. To prevent that issue, do not Step over PLL setup instructions do not set breakpoints right after PLL setup instructions make sure that any dual-port access is disabled during PLL setup disable terminal functionality during PLL setup
NEXUS-MPC56X Different Address Space for BDM vs. Nexus	**My Chip Select Setup works with a BDM debugger, but with a Nexus debugger the CS Setup does not work properly. What is the reason for?** If the upper addresses of the available address space are used to distinguish between the different chip select lines of the MPC56x, one must be aware that Nexus trace messages and dual ported memory access uses 25 address lines only (restricted by the Nexus aux. port protocol). A BDM-Debugger however, uses the full address space of 32 address lines. The only way to access full address space is to use the option "SYStem.Option HighMemory ON". Than all debugger accesses will be handled by BDM instructions in a Nexus message frame. In this case the CPU must be stopped in any case to access the memory. Bear in mind, that the trace reconstruction can not work properly in this case, due to the fact, that the address space in the trace messages can not be extended.

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NEXUS-MPC56X External Watchdog timer	**Why does the debugger not work on my target with an external watch-dog timer?** In general, all watch dog timers (WDT) in the system must be disabled anyhow. The debugger SW needs to initialize the Nexus interface of the device and must do other settings. Also it takes some time to start a user program. If a WDT pulls Reset before it can be disabled, the debugger SW has no chance to finish initialization. The device internal WDT will be disabled by the debugger SW during startup automatically. An external WDT must be turned off by HW. This is very important, because normally a batch job (Practice) sequence is too slow to do it in time by SW. The only chance to disable an external WDT by SW is to use an appropriate user program on the target which will be started by SYSTEM.STANDBY. This is the fastest method to start a user program out of Reset.
NEXUS-MPC56X MDI/MDO Lines Disconnected in MDO2 Mode	**Do MDI/MDO lines have to be disconnected from Nexus port in MDO2 mode?** Normally the only line which must be disconnected is MDI1. MDO 7..2 are input lines anyway and don't need to be disconnected. But it is recommended and usually done by the small PCB.
NEXUS-MPC56X Nexus Debug Port Fail	**Why do I get the error message "Emulator debug port fail"?** This is a global nexus protocol error . There are different reasons for this error message: Nexus message access timeout MCKO clock is missing general connector problems
NEXUS-MPC56X Nexus Probe (MNAD_x) Front Connector	**What is the pinout and the meaning of the Nexus Probe Front Connector? (MNAD_x)** Please refer to the pdf file. http://www.lauterbach.com/faq/frontjumperpinoutmbmad.pdf Pinout for MBMAD front connector

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NEXUS-MPC56X Port Replacement Feature	**Is the port replacement feature supported?** We don't expect to support the port replacement feature. It's made to use the same pins for Nexus and for the application when using an 80 pin connector. But device manufacturers don't seem to have plans to support this feature.
NEXUS-MPC56X Realtime Recording by NEXUS	**Can there be a delay between the time of a message is entered into the NEXUS message queue and the time of this message is sampled in the trace?** Yes, there can be a delay between the time of a message is entered into the NEXUS message queue (max. 8 entries) and the time of this message is sampled into the trace and marked with a time stamp. Delay due to different priorities of messages NEXUS messages have different priorities. High priority messages are output first. High priority messages are for example Invalid Messages. Data or Program messages have a low priority. The delay is not predictable. Delay due to the filling degree of the NEXUS queue If the NEXUS queue is nearly full when a message is entered, it take more time until the message is output. The delay is not predictable. Delay due to port width If a small NEXUS model is used it takes more time to output a message then on a large NEXUS model. The delay is predictable. Delay due to message portion collector in the NEXUS debugger A message can be 16, 24, 32 ... bit long. The NEXUS port has a width of 2 or 8 bit. So the NEXUS debugger has to wait until the complete message is output. When the NEXUS debugger received the full message, the message is sampled into the trace buffer and marked with a time stamp.
NEXUS-MPC56X Required Slot for NEXUS Preprocessor	**Which slot on the PowerTrace is used for the NEXUS adapter?** For the Motorola MPC56x family slot C has to be used.

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NEXUS-MPC56X TPU Registers are all Reset to Zero	**What do I have to consider if I want to debug the TPU?** To debug the TPU the CPU has to enter the test mode. An example is given in demo\powerPC\etc\tpu.cmm on the TRACE32 software CD. http://www.lauterbach.com/faq/tpu.cmm Demo
NEXUS-MPC56X Trace Impacts , Full trace settings	**Are there impacts using Nexus trace ? What are the right settings to get full trace?** Refer to the Motorola's AN http://www.lauterbach.com/faq/pages_from_nexus08oct20011.pdf AN by Motorola
NEXUS-MPC56X Usage of Nexus-pins or IO-pins	**Can the multi function pins (Nexus or I/O) be usesed as I/O during Nexus debugging?** No, they can't. When Nexus port is active the I/O function of the multi function pins will be disabled. If you prefer to debug and to use these I/O pins at a time you need to connect the additional BDM debug cable (no trace capability; extra charge) to PowerTrace instead of the Nexus preprocessor.
NEXUS-MPC56X Usage of the Terminal with NEXUS	**How is the terminal supposed to be used on nexus?** It works like dual port memory. So SingleE and BufferE are prefered modes. READPIPE and WRITEPIPE can connect the "host side"of the terminal to a named pipe on the host to talk to another application (not nexus specific).

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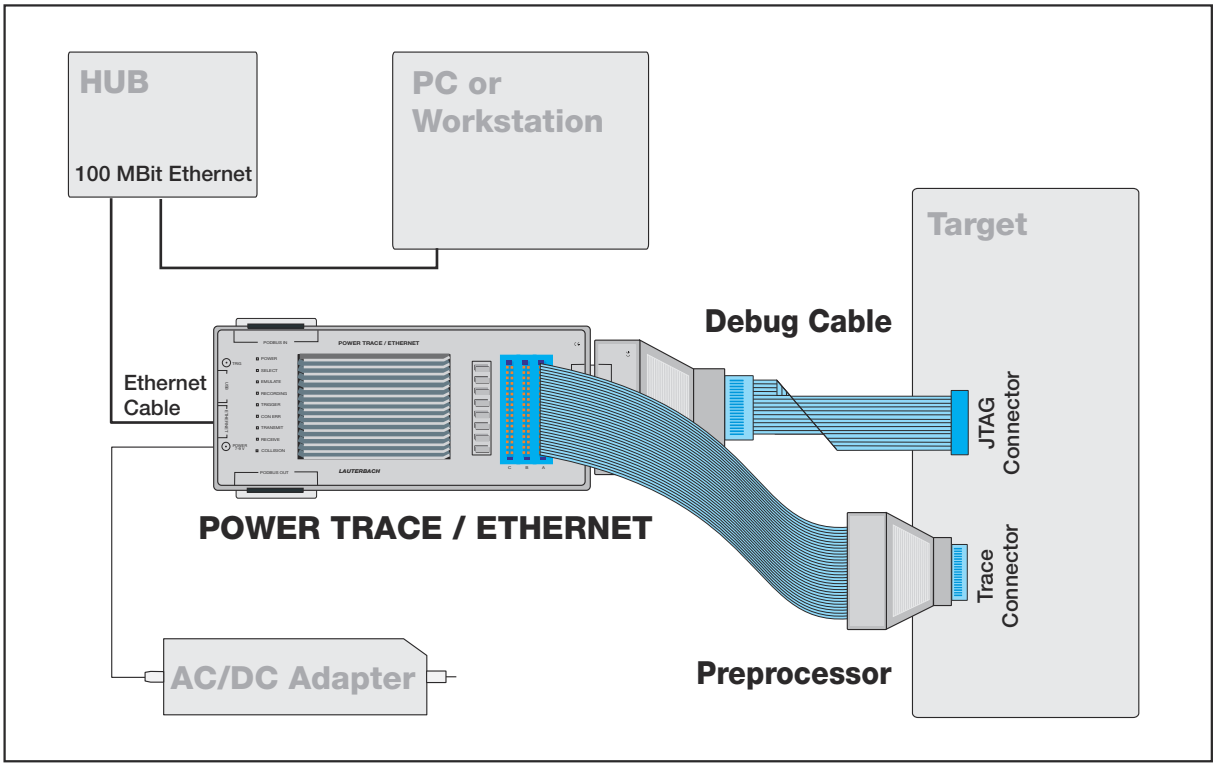

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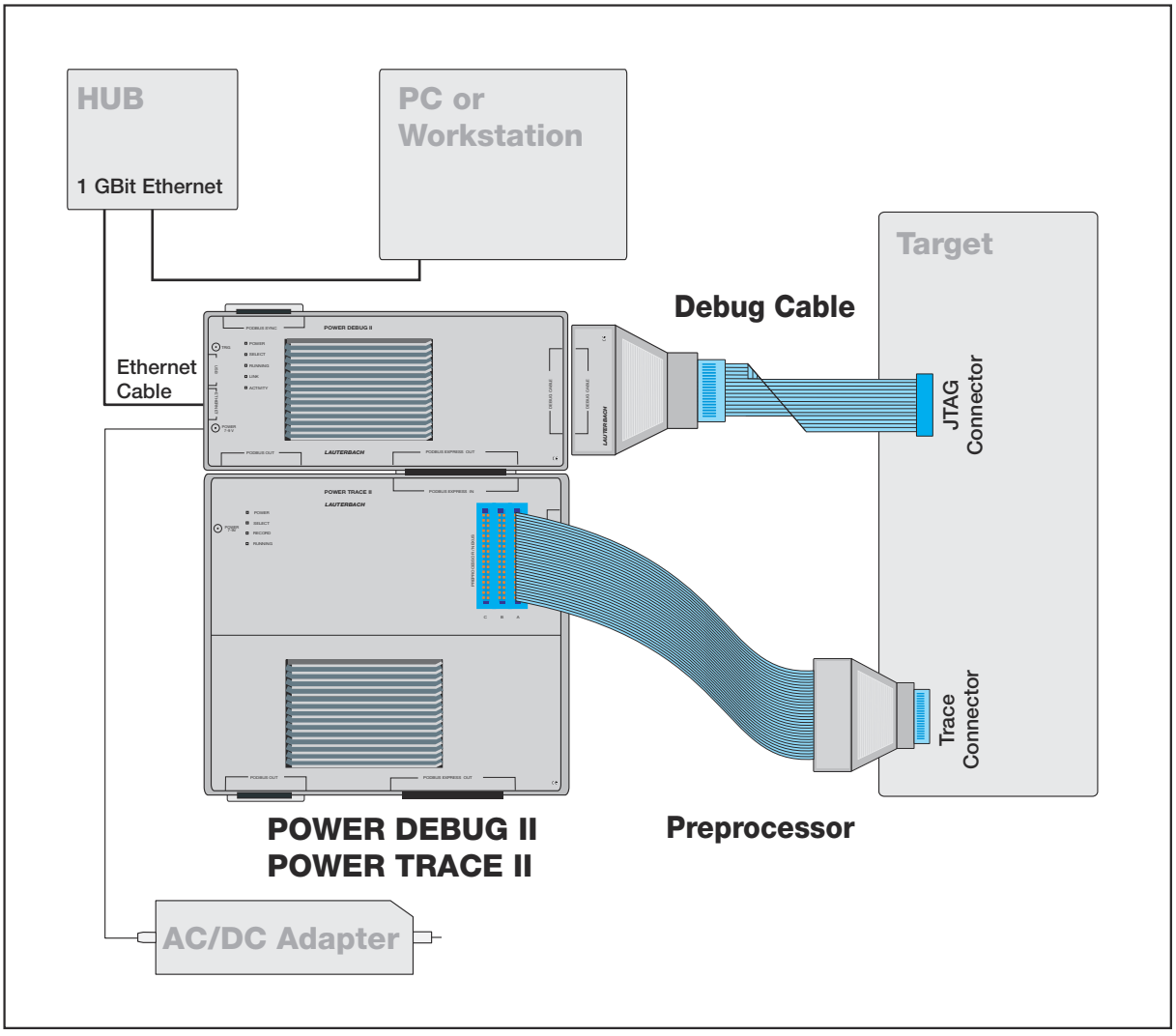

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Breakpoints

There are two types of breakpoints available: software breakpoints (SW-BP) and on-chip breakpoints (HW-BP).

Software Breakpoints

Software breakpoints are the default breakpoints on instructions. Software breakpoints can be set to any instruction address in RAM and after some preparations also to instructions in FLASH. For more information, refer to the command **FLASH.AUTO**.

There is no restriction in the number of software breakpoints. Please consider that increasing the number of software breakpoints will reduce the debug speed.

On-chip Breakpoints

The following list gives an overview of the usage of the on-chip breakpoints by TRACE32:

- **CPU family**
- **On-chip breakpoints:** Total amount of available on-chip breakpoints.
- **Instruction breakpoints:** Number of on-chip breakpoints that can be used for Program breakpoints.
- **Read/write breakpoints:** Number of on-chip breakpoints that can be used as Read or Write breakpoints.
- **Data breakpoints:** Number of on-chip data breakpoints that can be used to stop the program when a specific data value is written to an address or when a specific data value is read from an address.

CPU Family	On-chip Breakpoints	Instruction Breakpoints	Read/write Breakpoints	Data Breakpoints
MPC500/800	4 Instruction 2 Read/Write	4	2	2

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On-chip Breakpoints on InstructionsROM or FLASH

If a breakpoint is set to an instruction, a software breakpoint is used by default. If your code is in FLASH, ROM etc. you can advise TRACE32 to automatically use on-chip breakpoint for specific address ranges by using the command **MAP.BOnchip** <range>.

On-chip Breakpoints on Read or Write Accesses

On-chip breakpoints are always used, if a Read or Write breakpoint is set. For the MPC5xx/8xx it is also possible to define a specific data value. Refer to the **Break.Set** command for more information.

Example for Breakpoints

Assume you have a target with FLASH from `0` to `0xFFFFF` and RAM from `0x100000` to `0x11FFFF`. The command to configure TRACE32 correctly for this configuration is:

```
Map.BOnchip 0x0--0x0FFFFF
```

The following breakpoint combinations are possible.

Software breakpoints:

```
Break.Set 0x100000 /Program                          ; Software Breakpoint 1
Break.Set 0x101000 /Program                          ; Software Breakpoint 2
Break.Set 0xx /Program                               ; Software Breakpoint 3
```

On-chip breakpoints:

```
Break.Set 0x100 /Program                             ; On-chip Breakpoint 1
Break.Set 0x0ff00 /Program                           ; On-chip Breakpoint 2
Break.Set   flags /Write                             ; On-chip Breakpoint 3
Var.Break.Set \flags[3] /Write /DATA.Byte 0x1        ; On-chip Breakpoint 4
```

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Simultaneous FLASH Programming for MPC555

Simultaneous programming of the internal FLASH is supported for the masks K1, K2, K3 and M of the MPC555.

The MPC555 supports simultaneous programming of all 14 flash modules.

- 8 64-byte pages in the 8 blocks of FLASH module A
- 6 64-byte pages in the 6 blocks of FLASH module B

Using simultaneous FLASH programming is up to 7 times faster!

Programming Procedure

1. Load the application program into the virtual memory of TRACE32-ICD.

   For the simultaneous FLASH programming the code can not directly be loaded from the host. The code has to be loaded into the virtual memory (VM) of TRACE32-ICD first.

   TRACE32-PowerView can recognize empty 64-byte pages and skip them while programming. For this reason the virtual memory should be initialized with 0xff.

   ```
   ; initialize the virtual memory of TRACE32-ICD with 0xff
   Data.Set VM:<start_address_internal_flash>++0x6ffff %Long
   0xffffffff

   ; load the code for the internal FLASH into the virtual memory
   Data.LOAD.Elf <file_name> <start_address_internal_flash>++0x6ffff /
   VM
   ```

2. Start the simultaneous programming.

   ```
   FLASH.MultiProgram <start_address_internal_flash>++0x6ffff
   ```

If your application program also contains code for the external FLASH, this code has to be loaded separately.

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Memory Classes

The following memory classes are available:

Memory Class	Description
P	Program
D	Data
SPR	Special Purpose Register
IC	Instruction Cache (MPC8xx only)
DC	Data Cache (MPC8xx only)
NC	No Cache (only physically memory)

If the cache is disabled, memory accesses to the memory classes IC or DC are realized by TRACE32-ICD as reads and writes to physical memory.

Memory Coherency MPC8xx

Memory coherency on access to the following memory classes. If data will be set to DC, IC, NC, D or P the D-Cache, I-Cache or physical memory will be updated.

	D-Cache	I-Cache	Physical Memory
DC:	Yes	No	Yes
IC:	No	Yes	Yes
NC:	No	No	Yes
D:	Yes	Yes	Yes
P:	Yes	Yes	Yes

See also **SYStem.Option ICREAD** and **SYStem.Option DCREAD.**

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MPC555/MPC553 Pin Multiplexing

CLKOUT	Always required.
A8..A29	Are always required.
D0..D11	Are required for tracing in compressed mode.
WR	Is required.
STS	Is not present when SIUMCR.DBGC== 00. In this case it is assumed that the program trace show cycle for indirect change of flow is appearing directly at the same clock where the indirect change of flow is shown. This should be always the case when running only with internal memories and having only indirect program show cycles active (no data cycles or data show cycles).
PTR	Is not present when SIUMCR.GPC !=00. In this case ALL program cycles are assumed to be program trace cycles. This is always the case when the program is running from internal memory and only indirect show cycles are enabled. When external program memory is used the trace may not be able to take the correct cycle as target for the indirect branch.
AT(2)	Is taken from the WE2/AT2 line when SIUMCR.ATWC==1 (AT0-3 lines enabled) or taken from the dedicated AT(2) line when SIUMCR.ATWC==0 (WE0-3 lines enabled) and SIUMCR.MLRC ==x1 (AT(2) function enabled). When non of the two variants is possible the debugger will assume that ALL cycles are program cycles (no data cycles). The program flow trace will not be affected by this, as long as the PTR line is available. When the AT(2) and PTR lines are both not available the trace will only work when the code is running from internal memory and only “indirect change of flow” show cycles are enabled.
VF0,VF1	Is taken from SIU when SIUMCR.DBGC==10, otherwise from the MIOS pins. MIOS must be configured when MIOS pins are used. If none of the pins are available then the program flow trace will not work. Direct cycle tracing in fully serialized mode with show cycles for all cycles will still work.
VFLS0,VFLS1	Is taken from SIU when SIUMCR.DBGC==x0, otherwise from the MIOS pins. MIOS must be configured when MIOS pins are used.
LWPx, IWPx	Optional lines. Only used when selective tracing features should be used.

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Target is not running with trace attached

Some trace adapters use drivers with “Bus Hold” feature. This resistor (about 20 k) can pull the lines connected to the trace to VCC or Ground. If the target is using high impedance resistors to select a specific level for the reset configuration it may not work. In this case make either the resistors on the target smaller or disable the external reset configuration. Pulling down the TS line may also cause such effects. Use a pull-up resistor (about 10 k) in this case.

Nothing recorded (number of records in Analyzer.state window remains 0)

Check that CLKOUT is available on the trace probe. Check that VFLS0 and VFLS1 are correctly configured.

No cycle information displayed in Analyzer.List

Check the TS and STS signals.

Cycle type information in Analyzer.List is wrong

Check the RW and AT lines (CT lines for MPC50x).

Address information is wrong for DRAM accesses

Define DRAM areas with **MAP.DMUX** command.

Flowtrace (Analyzer.List /FT) gives no useful results

Make sure that indirect branch program trace cycles are enabled (**SYStem.Option ICTL IND**). Check that PTR signal is correctly recorded in trace. Check for presence of VF0, VF1 and VF2 signals. Make sure that program has executed an indirect branch while sampling data for the trace.

Used Options for RiscTrace

- **SYSTEM.OPTION NODATA** ON /OFF
- **SYSTEM.OPTION SIUMCR** ON /OFF
- SIUMCR Register [DBGC,GPC] (Peripheral Window)

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SYStem.BdmClock — Define the BDM clock speed

Format:	**SYStem.BdmClock** <*rate*>
<*rate*>:	**EXT/4 | EXT/8 | EXT/16 |** <*fixed*>
<*fixed*>:	**1MHz … 20MHz**

Selects the frequency for the debug interface. A fixed frequency or an divided external clock can be used.

SYStem.CONFIG — Configure debugger according to target topology

There are no multicore capable CPUs available at the moment.

SYStem.CPU — Select CPU type

Format:	**SYStem.CPU** <*cpu*>
<cpu>:	**MPC5xx | MPC8xx**

Selects the processor type.

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Format: **SYStem.CpuAccess** <mode>

<mode>: **Enable | Denied | Nonstop**

Enable Enable performs an update of the memory displayed in the TRACE32 window. Therefore the debugger stops the program execution about 10 times/s, switches to debug mode, updates the memory and restarts the program execution afterwards.
Each short stop takes 1 … 100 ms depending on the speed of the debug interface and on the size of the read/write accesses required.
The run-time memory access has to be activated for each window by using the memory class E: (e.g. Data.dump E:0x100) or by using the format option %E (e.g. Var.View %E var1).

Denied No memory read or write is possible while the CPU is executing the program.

Nonstop Nonstop ensures that the program execution can not be stopped and that the debugger doesn't affect the real-time behavior of the CPU.
Nonstop reduces the functionality of the debugger to:

- run-time access to memory and variables
- trace display

The debugger inhibits the following:

- to stop the program execution
- all features of the debugger that are intrusive (e.g. spot breakpoints, performance analysis via StopAndGo, conditional breakpoints etc.)

SYStem.MemAccess Real-time memory access (non-intrusive)

Format: **SYStem.MemAccess Denied**

Denied No run-time memory access is possible for the MPC5xx/8xx family.

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Format:	**SYStem.Mode** <*mode*>
<*mode*>:	**Down** **StandBy** **Up**

Select target reset mode.

Down Disables the debugger.

StandBy This mode is used to start debugging from power-on. The debugger will wait until power-on is detected, then bring the CPU into debug mode, set all debug and trace registers and start the CPU. In order to halt the CPU at the first instruction, place an on-chip breakpoint to the reset address (Break.Set 0x100 /Onchip)

Up Resets the CPU, enables the debug mode and stops the CPU at the first opfetch (reset vector). All register are set to the default value.

Go Resets the target with debug mode enabled and prepares the CPU for debug mode entry. After this command the CPU is in the system.up mode and running. Now, the processor can be stopped with the break command or until any break condition occurs.

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SYStem.LOADVOC — Load vocabulary for code compression

Format:	**SYStem.LOADVOC** <*file*>

Load vocabulary for code compression. This is usually not required, since the vocabulary is already in the ELF file.

FLASH.MultiProgram — Simultaneous programming of on-chip FLASH

Available on:	**MPC555 (K1, K2, K3)**
Format:	**FLASH.MultiProgram** <*range*>

Allows simultaneous programming of the internal FLASH. For a complete description of the programming procedure see **Simultaneous FLASH Programming for MPC555**.

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Format: **SYStem.Option BRKNOMSK [ON | OFF]**

The CPU handles debug events similar to exceptions. When a debug event (normally a break) OR an exception occurs, the CPU copies the MSR (Machine Status Register) into SRR1 (Machine Status Save/ Restore Register 1) and the IP (Instruction Pointer) into SRR0 (Machine Status Save/Restore Register 1). This means, that after an exception occurred, the old values of IP and MSR are as backup in the SRR0 and SRR1 registers. If now a break happens, these values will be overwritten by the new MSR and IP values. So, it is possible to return to the exception routine and stop the processor, **but it's not possible to return to the main program and continue the user application!** The status after the start of the exception routine is called non recoverable state.

If one wants to break in a non recoverable state, you must switch the option BrkNoMsk to on.

ON The program execution can be stopped by a breakpoint even if the processor is in a non-recoverable state. Since the debug exception overwrites SRR0 and SRR1 it is not advisable to continue the debugging process.

OFF The program execution is not stopped as long as the processor is in a non-recoverable state (RI bit cleared in the Machine Status register).

SYStem.Option CCOMP Enable code compression

Format: **SYStem.Option CCOMP [ON | OFF]**

If the code compression unit of the MPC5xx is used, this option must be switched on before the program is loaded. Then correct disassembly is possible.

SYStem.Option CLEARBE Clear MSR[BE] on step/go

Format: **SYStem.Option CLEARBE [ON | OFF]**

If the option CLEARBE is switched on, the BE bit of the MSR register will be cleared before every Go or Step.

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Available on:	**MPC505, MPC509**
Format:	**SYStem.Option CSBTOR [<value>]** **SYStem.Option CSBTSBOR [<value>]** **SYStem.Option CSBTBAR [<value>]** **SYStem.Option CSBTSBBAR [<value>]** **SYStem.Option CS0OR [<value>]** **SYStem.Option CS1OR [<value>]** **SYStem.Option CS2OR [<value>]** **SYStem.Option CS3OR [<value>]** **SYStem.Option CS4OR [<value>]** **SYStem.Option CS5OR [<value>]** **SYStem.Option CS6OR [<value>]** **SYStem.Option CS7OR [<value>]** **SYStem.Option CS8OR [<value>]** **SYStem.Option CS9OR [<value>]** **SYStem.Option CS10OR [<value>]** **SYStem.Option CS11OR [<value>]** **SYStem.Option CS0BAR [<value>]** **SYStem.Option CS1BAR [<value>]** **SYStem.Option CS2BAR [<value>]** **SYStem.Option CS3BAR [<value>]** **SYStem.Option CS4BAR [<value>]**

For the flow trace functionality, it is necessary for the software to know the settings of the CS unit. The values of these options must be the same values as the register values of the chip.

SYStem.Option DCREAD Use DCACHE for data read

Format:	**SYStem.Option DCREAD [ON | OFF]**

ON (Default) If data memory is displayed (memory class D:) the memory contents from the D-cache is displayed if the D-cache is valid. If D-cache is not valid the physical memory will be read. Typical command to display data memory are: Data.dump, Var.Watch, Var.View.

OFF If data memory is displayed (memory class D:) the memory contents from the physical memory is displayed.

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Format: **SYStem.Option FAILSAVE [ON | OFF]**

The debug interface of the MPC8xx and MPC5xx returns the fatal error emulation debug port fail, when reading incorrect communication data from the debug port. With this option, it is possible to suppress this debug port fail, and recover the communication. This helps debugging in noisy environment.

SYStem.Option FreezePin Use alternative signal on the BDM connector

Available on: **MPC8xx**

Format: **SYStem.Option FreezePin [ON | OFF]**

As default, this option is off and the debugger set all necessary setting for the SIMCR register for the most frequently used **option A**. (VFLS0/1 pins are connected to BDM connector pin 1 and 6). The SYStem.Option.FreezePin can prevent the debugger for resetting/overwriting the SIMCR register to the default settings.

If **option B** is used (FREEZE pin is connected to the BDM connector) this SYStem.Option.FreezePin must be switched on.

NOTE: For the MPC5xx family all necessary configuration for the correct BDM pin setting have to be done in the RSTCONF word.

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Format: **SYStem.Option IBUS [<Value>]**

With this option, you can set the instruction fetch show cycle and serialize control bits of the IBUS support control register.

SERALL All fetch cycles are visible on the external bus. In this mode the processor is fetch serialized. Therefore the processor performance is much lower then working in regular mode.

SERCHG All cycles that follow a change in the program flow are visible on the external bus. In this mode the processor is fetch serialized. Therefore the processor performance is much lower then working in regular mode.

SERIND All cycles that follow an indirect change in the program flow are visible on the external bus. In this mode the processor is fetch serialized. Therefore the processor performance is much lower then working in regular mode.

SERNONE In this mode the processor is fetch serialized. Therefore the processor performance is much lower then working in regular mode. No information about the program flow is visible on the external bus.

CHG All cycles that follow a change in the program flow are visible on the external bus. The performance degradation is small here.

IND All cycles that follow an indirect change in the program flow are visible on the external bus. The performance degradation is small here.
This setting is recommended if a preprocessor for MPC500/800 is used.

NONE No show cycles are performed. (Recommended when only a BDM debugger is used.)

RESERVED Should not be used.

SYStem.Option ICFLUSH Flush branch target cache before program start

Format: **SYStem.Option ICFLUSH [ON | OFF]**

Invalidates the instruction cache and flush the data cache before starting the target program (Step or Go). This is required when the CACHEs are enabled and software breakpoints are set to a cached location.

MPC5xx: Flushes the Instruction Prefetch Queue before starting the program execution by `Step` or `Go`

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Format: **SYStem.Option ICREAD [ON | OFF]**

ON If program memory is displayed (memory class P:) the memory contents from the I-cache is shown if the I-cache is valid. If I-cache is not valid the physical memory will be read. Typical command for program memory display are: Data.List, Data.dump.

OFF (Default) If program memory is displayed (memory class P:) the memory contents from the physical memory is displayed.

SYStem.Option IMASKASM Disable interrupts while single stepping

Format: **SYStem.Option IMASKASM [ON | OFF]**

Default: OFF.

If enabled, the interrupt mask bits of the CPU will be set during assembler single-step operations. The interrupt routine is not executed during single-step operations. After single step the interrupt mask bits are restored to the value before the step.

SYStem.Option IMASKHLL Disable interrupts while HLL single stepping

Format: **SYStem.Option IMASKHLL [ON | OFF]**

Default: OFF.

If enabled, the interrupt mask bits of the cpu will be set during HLL single-step operations. The interrupt routine is not executed during single-step operations. After single step the interrupt mask bits are restored to the value before the step.

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Format: **SYStem.Option LittleEnd [ON | OFF]**

With this option data is displayed little endian style.

Normally, the PowerPC debugger displays data big endian style.

SYStem.Option MMUSPACES Support multiple address spaces

Format: **SYStem.Option MMUSPACES [ON | OFF]**

Enables the usage of the MMU to support **multiple** address spaces. The command should not be used if only one translation table is used. Enabling the option will extend the address scheme of the debugger by a 16 bit memory space identifier. The option can only be enabled when there are no symbols loaded. This option is needed for operating systems that run several applications at the same virtual address space (e.g. Linux). The debugger uses this 16 bit memory space identifier to assign debug symbols to the memory space of the according process.

SYStem.Option NODATA The external data bus is not connected to trace

Format: **SYStem.Option NODATA [ON | OFF]**

ON No external data bus is connected to the trace connector.

OFF (Default) The external data bus is connected to the trace connector.

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Format: **SYStem.Option NOTRAP [ON | OFF]**

ON With this setting the TRAP exception is no longer used for software breakpoints. UNDEF 0 is used instead.
Use the command **TrOnchip.Set PRIE OFF**. With this setting the debug mode is no longer entered when a TRAP occurs. See also the Debug Enable Register in you processor manual.
Now your application can handle the TRAP instruction.

OFF (Default) The TRAP exception is used for software breakpoints.

SYStem.Option OVERLAY

Enable overlay support

Format: **SYStem.Option OVERLAY** [**ON** | **OFF** | **WithOVS**]

Default: OFF.

ON: Activates the overlay extension and extends the address scheme of the debugger with a 16 bit virtual OverlayID. Addresses therefore have the format `<OverlayID>:<address>`. This enables the debugger to handle overlayed program memory.

OFF: Disables support for code overlays.

WithOVS: Like option **ON**, but also enables support for software breakpoints. This means that TRACE32 writes software breakpoint opcodes both to the *execution area* (for active overlays) and to the *storage area*. In this way, it is possible to set breakpoints into inactive overlays. Upon activation of the overlay, the target's runtime mechanisms copies the breakpoint opcodes to execution area. For using this option, the storage area must be readable and writable for the debugger.

```
SYStem.Option OVERLAY ON
Data.List 0x2:0x11c4                    ; Data.List <OverlayID>:<address>
```

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SYStem.Option PPCLittleEnd — Control for PPC little endian

Format: **SYStem.Option LittleEnd [ON | OFF]**

Normally, the PowerPC debugger displays data big endian style.

With this option data is displayed in PPC little endian style.

SYStem.Option SCRATCH — Scratch for FPU access

Format: **SYStem.Option SCRATCH** <address> **| AUTO**

Reading the FPU registers of the MPC5xx requires two memory words in target memory. This option defines which location is used. The content of the memory location will be restored after use. If AUTO is used, two memory words of the on-chip RAM are used for reading the FPU registers.

SYStem.Option SIUMCR — SIUMCR setting for the trace

Format: **SYStem.Option SIUMCR** [<**value**>]

In order to trace the program and data flow, it is necessary for the TRACE32 software to know the settings of some peripheral pins. The value of this option must be the same value as the SIUMCR register of the chip.

SYStem.Option SLOWLOAD — Alternative data load algorithm

Format: **SYStem.Option SLOWLOAD [ON | OFF]**

The debug interface of the MPC8xx and MPC5xx has a special mode for fast download of 32 bit data. For some older versions of the chips, it might be necessary to switch to a slower download mode to get proper results.

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Format: **SYStem.Option SLOWRESET [ON | OFF]**

After the debugger resets the CPU (e.g. via SYStem.Up), the debugger senses $\overline{\texttt{HRESET}}$ for 2 … 3 s before an error message is displayed.

SYStem.Option WATCHDOG Enable software watchdog after SYStem.Up

Format: **SYStem.Option WATCHDOG [ON | OFF]**

If this option is switched off, the watchdog timer of the CPU is disabled after the SYStem.Up.

Otherwise the watchdog will be periodically reset by the debugger. **Software Watchdog Timer (SWT) —** The SWT asserts a reset or non-maskable interrupt (as selected by the system protection control register) if the software fails to service the SWT for a designated period of time (e.g, because the software is trapped in a loop or lost). After a system reset, this function is enabled with a maximum time-out period and asserts a system reset if the time-out is reached. The SWT can be disabled or its time-out period can be changed in the SYPCR. Once the SYPCR is written, it cannot be written again until a system reset.

Software Watchdog Timer (SWT) — The SWT asserts a reset or non-maskable interrupt (as selected by the system protection control register) if the software fails to service the SWT for a designated period of time (e.g, because the software is trapped in a loop or lost). After a system reset, this function is enabled with a maximum time-out period and asserts a system reset if the time-out is reached. The SWT can be disabled or its time-out period can be changed in the SYPCR. Once the SYPCR is written, it cannot be written again until a system reset.

SYStem.state Display SYStem window

Format: **SYStem.state**

Displays the SYStem window.

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MMU.DUMP — Page wise display of MMU translation table

Format: **MMU.DUMP** *<table>* [*<range>* | *<addr>* | *<range>* *<root>* | *<addr>* *<root>*]
MMU.<table>.dump (deprecated)

<table>: **PageTable**
KernelPageTable
TaskPageTable *<task>*
and CPU specific tables

Displays the contents of the CPU specific MMU translation table.

- If called without parameters, the complete table will be displayed.
- If the command is called with either an address range or an explicit address, table entries will only be displayed, if their **logical** address matches with the given parameter.

The optional <root> argument can be used to specify a page table base address deviating from the default page table base address. This allows to display a page table located anywhere in memory.

PageTable — Display the current MMU translation table entries of the CPU.
This command reads all tables the CPU currently used for MMU translation and displays the table entries.

KernelPageTable — Display the MMU translation table of the kernel.
If specified with the **MMU.FORMAT** command, this command reads the MMU translation table of the kernel and displays its table entries.

TaskPageTable — Display the MMU translation table entries of the given process.
In MMU based operating systems, each process uses its own MMU translation table. This command reads the table of the specified process, and displays its table entries.
See also the appropriate **OS awareness manuals**: RTOS Debugger for <x>.

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CPU specific tables:

ITLB	Displays the contents of the Instruction Translation Lookaside Buffer.
DTLB	Displays the contents of the Data Translation Lookaside Buffer.

MMU.List — Compact display of MMU translation table

Format:	**MMU.List** [*<table>* [*<range>* | *<address>*]] **MMU.<table>.List (deprecated)**
<table>:	**PageTable** **KernelPageTable** **TaskPageTable** *<task>*

Lists the address translation of the CPU specific MMU table. If called without address or range parameters, the complete table will be displayed.

If called without a table specifier, this command shows the debugger internal translation table.
See **TRANSlation.List**.

If the command is called with either an address range or an explicit address, table entries will only be displayed, if their **logical** address matches with the given parameter.

PageTable	List the current MMU translation of the CPU. This command reads all tables the CPU currently used for MMU translation and lists the address translation.
KernelPageTable	List the MMU translation table of the kernel. If specified with the **MMU.FORMAT** command, this command reads the MMU translation table of the kernel and lists its address translation.
TaskPageTable	List the MMU translation of the given process. In MMU based operating systems, each process uses its own MMU translation table. This command reads the table of the specified process, and lists its address translation. See also the appropriate **OS awareness manuals**: RTOS Debugger for <x>.

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Format: **MMU.SCAN** *<table>* [*<range>* *<address>*]
MMU.<table>.SCAN (deprecated)

<table>: **PageTable**
KernelPageTable
TaskPageTable *<task>*
ALL
and CPU specific tables

Loads the CPU specific MMU translation table from the CPU to the debugger internal translation table. If called without parameters the complete page table will be loaded. The loaded address translation can be viewed with **TRANSlation.List**.

If the command is called with either an address range or an explicit address, page table entries will only be loaded if their **logical** address matches with the given parameter.

PageTable Load the current MMU address translation of the CPU.
This command reads all tables the CPU currently used for MMU translation, and copies the address translation into the debugger internal translation table.

KernelPageTable Load the MMU translation table of the kernel.
If specified with the **MMU.FORMAT** command, this command reads the table of the kernel and copies its address translation into the debugger internal translation table.

TaskPageTable Load the MMU address translation of the given process.
In MMU based operating systems, each process uses its own MMU translation table. This command reads the table of the specified process, and copies its address translation into the debugger internal translation table.
See also the appropriate **OS awareness manuals**: RTOS Debugger for <x>.

ALL Load all known MMU address translations.
This command reads the OS kernel MMU table and the MMU tables of all processes and copies the complete address translation into the debugger internal translation table.
See also the appropriate **OS awareness manuals**: RTOS Debugger for <x>.

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CPU specific tables:

ITLB	Loads the instruction translation table from the CPU to the debugger internal translation table.
DTLB	Loads the data translation table from the CPU to the debugger internal translation table.
TLB	Loads the translation table from the CPU to the debugger internal translation table.
TLB0	Loads the translation table 0 from the CPU to the debugger internal translation table.
TLB1	Loads the translation table 1from the CPU to the debugger internal translation table.
TLB2	Loads the translation table 2 from the CPU to the debugger internal translation table.

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MMU.TLB — Display MMU TLB entries

Format: **MMU.TLB** <*tlb*>

<*tlb*>: **IMMU**
DMMU

Displays a table of all MMU TLB entries of the specified TLB table.

MMU.TLBSCAN — Load MMU TLB entries

Format: **MMU.TLBSCAN**
MMU.TLBSCAN <*tlb*>

<*tlb*>: **IMMU**
DMMU

Loads the TLB table entries from the CPU to the debugger internal MMU table. If no TLB table is specified, both are scanned.

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TrOnchip.CONVert — Adjust range breakpoint in on-chip resource

Format: **TrOnchip.CONVert [ON | OFF]**

For on-chip-breakpoints see the **corresponding chapter**.

ON (default) — If all resources for the on-chip breakpoints are already used and if the user wants to set an additional on-chip breakpoint, TRACE32 converts an on-chip breakpoint set to a short address range (max. 4 bytes) to a single address breakpoint to free additional resources.

OFF — If all resources for the on-chip breakpoints are already used and if the user wants to set an additional on-chip breakpoint, an error message is displayed.

Example:

```
TrOnchip.Convert ON

Break.Set 0x100++0x4 /Write      ; Set a write breakpoint to the
                                 ; address range 0x100++0x4

Break.Set 0x800 /Write           ; Set a write breakpoint to the address
                                 ; 0x800. The first set breakpoint is
                                 ; reduced to address 0x100
```

TrOnchip.DISable — Disable NEXUS trace register control

Format: **TrOnchip.DISable**

Disables NEXUS register control by the debugger. By executing this command, the debugger will not write or modify any registers of the NEXUS block. This option can be used to manually set up the NEXUS trace registers. The NEXUS memory access is not affected by this command. To re-enable NEXUS register control, use command **TrOnchip.ENable**. Per default, NEXUS register control is enabled.

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Format: **TrOnchip.ENable**

Enables NEXUS register control by the debugger. By default, NEXUS register control is enabled. This command is only needed after disabling NEXUS register control using **TrOnchip.DISable**.

TrOnchip.G/H Define data selector

Format: **TrOnchip.G.Value** <*hexmask*> | <*float*>
TrOnchip.H.Value <*hexmask*> | <*float*>
TrOnchip.G.Size [Byte | Word | Long]
TrOnchip.H.Size [Byte | Word | Long]
TrOnchip.G.Match [OFF | EQ | NE | GT | LT | GE | LE]
TrOnchip.H.Match [OFF | EQ | NE | GT | LT | GE | LE]

Defines the two data selectors of the MPC500/800 family.

OFF	Off
EQ	Equal
NE	Not equal
LE	Lower equal
GE	Greater equal
LT	Lower then
GT	Greater then
ULE	Unsigned lower equal
UGE	Unsigned greater equal
ULT	Unsigned lower then
UGT	Unsigned greater then

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Example: Stop the program execution if a value between 0x50 and 0x70 is written to the variable vint.

```
Var.Break.Set vint /Alpha    ; Set a breakpoint of the type Alpha to vint

; Program the first L-Bus watchpoint

TrOnchip.RESet               ; Reset on-chip trigger unit

TrOnchip.LW0 LBUS Alpha      ; The addresses marked with Alpha
                             ; breakpoints define the L-Bus address

TrOnchip.LW0.CYcle Write     ; The L-Bus cycle is write

TrOnchip.LW0.Data GANDH      ; The L-Bus data is a logical AND of data
                             ; selector G and H

; Program the data selector G

TrOnchip.G.Value 0x50        ; The value for G is 0x50

TrOnchip.G.Size Long         ; The access size is Long

TrOnchip.G.Match GT          ; The match is GreaterThan

; Program the data selector H

TrOnchip.H.Value 0x70        ; The value for H is 0x70

TrOnchip.H.Size Long         ; The access size is Long

TrOnchip.H.Match LT          ; The match is LowerThan
```

TrOnchip.IWx.Count — Event counter for I-Bus watchpoint

Format: **TrOnchip.IW0.Count** <*count*>
TrOnchip.IW1.Count <*count*>

The occurrence of the specified I-Bus event can be counted.

Example: Stop the program execution after 100. entries to INT5.

```
Break.Set INT5 /Alpha        ; Set an Alpha breakpoint to the entry of
                             ; INT5

TrOnchip.RESet               ; Reset on-chip trigger unit
```

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```
TrOnchip.IW0.Ibus Alpha      ; The addresses marked with Alpha
                             ; breakpoints define the I-Bus address

TrOnchip.IW0.Count 100.      ; The I-Bus counter is set to 100.

Go
```

TrOnchip.IWx.Ibus — Instructions address for I-Bus watchpoint

Format: **TrOnchip.IW0.Ibus** <*selector*>
TrOnchip.IW1.Ibus <*selector*>

<*selector*>: **OFF**
Alpha
Beta
Charly
Delta
Echo

Define the instruction for the I-Bus watchpoint.

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Format: **TrOnchip.IW0.Watch [OFF | ON]**
TrOnchip.IW1.Watch [OFF | ON]

ON A pulse is generated on IWP0/IWP1/IWP2/IWP3 if the I-Bus watchpoint is hit. The processor pins IWP0/IWP1/IWP2/IWP3 serve multiple functions. Please check your target hardware to find out which pin can be used for the trigger pulse. The smallest pulse length is one clock cycle.

OFF The program execution is stop on a hit of the L-Bus watchpoint.

Example: Generate a pulse on IW0 when the function func5 is entered. Generated a pulse on IW1 on the exit of func5.

```
Break.Set func5 /Alpha              ; Set an Alpha breakpoint to the entry
                                    ; of func5

Break.Set v.end(func5)-3 /Beta      ; Set a Beta breakpoint to the exit of
                                    ; func5

TrOnchip.RESet                      ; Reset the on-chip trigger unit

TrOnchip.IWO.Ibus Alpha             ; The addresses marked with Alpha
                                    ; breakpoints define the Ibus address

TrOnchip.IWO.Watch ON               ; Generate a pulse on IWP0 when IW0 is
                                    ; hit

TrOnchip.IW1.Ibus Beta              ; The addresses marked with Beta
                                    ; breakpoints define the Ibus address

TrOnchip.IW1.Watch ON               ; Generate a pulse on IWP1 when IW1 is
                                    ; hit
```

TrOnchip.LW0.Count Event counter for L-Bus watchpoint

Format: **TrOnchip.LW0.Count** <*count*>
TrOnchip.LW1.Count <*count*>

The occurrence of the specified L-Bus event can be counted.

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Example: Stop the program execution after 100. write accesses to flags[3].

```
Var.Break.Set flags[3] /Alpha     ; Set an Alpha breakpoint to flags[3]

TrOnchip.RESet                    ; Reset on-chip trigger unit

TrOnchip.LW0.Lbus Alpha           ; The addresses marked with Alpha
                                  ; breakpoints define the L-Bus address

TrOnchip.LW0.CYcle Write          ; The L-Bus cycle is write

TrOnchip.LW0 Count 100.           ; The L-Bus counter is set to 100.

Go
```

TrOnchip.LW0.CYcle — Cycle type for L-Bus watchpoint

Format: **TrOnchip.LW0.CYcle** <*cycle*>
TrOnchip.LW1.CYcle <*cycle*>

<*cycle*>: **Read**
Write
Access

Define the cycle type for the L-Bus watchpoint.

TrOnchip.LW0.Data — Data selector for L-Bus watchpoint

Format: **TrOnchip.LW0.Data** <*selector*>
TrOnchip.LW1.Data <*selector*>

<*selector*>: **OFF**
G
H
GANDH
GORH

Define the data selector for the L-Bus watchpoint.

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Format: **TrOnchip.LW0.Ibus** <*selector*>
TrOnchip.LW1.Ibus <*selector*>

<*selector*>: **OFF**
Alpha
Beta
Charly
Delta
Echo

Define the instruction for the L-Bus watchpoint.

Example: Stop the program execution if func5 writes to flags[3].

```
Var.Break.Set func5 /Alpha        ; Set an Alpha breakpoint to the
                                  ; complete range of func5

Var.Break.Set flags[3] /Beta      ; Set a Beta breakpoint to flags[3]

TrOnchip.RESet                    ; Reset on-chip trigger unit

TrOnchip.LW0.Ibus Alpha           ; The addresses marked with Alpha
                                  ; breakpoints define the instruction
                                  ; address for LW0

TrOnchip.LW0.Lbus /Beta           ; The addresses marked with Beta
                                  ; breakpoints define the data address
                                  ; for LW0

TrOnchip.LW0.CYcle Write          ; The data cycle is write
```

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Format: **TrOnchip.LW0.Lbus** <*selector*>
TrOnchip.LW1.Lbus <*selector*>

<*selector*>: **OFF**
Alpha
Beta
Charly
Delta
Echo

Defines on which data address for the L-Bus watchpoint.

TrOnchip.LW0.Watch Activate L-Bus watchpoint pin

Format: **TrOnchip.LW0.Watch [OFF | ON]**
TrOnchip.LW1.Watch [OFF | ON]

ON A pulse is generated on LWP0/LWP1 if the L-Bus watchpoint is hit. The processor pins LWP0/LWP1 serve multiple functions. Please check your target hardware to find out which pin can be used for the trigger pulse. The smallest pulse length is one clock cycle.

OFF The program execution is stop on a hit of the L-Bus watchpoint.

TrOnchip.RESet Reset on-chip trigger unit

Format: **TrOnchip.RESet**

Reset the on-chip trigger unit.

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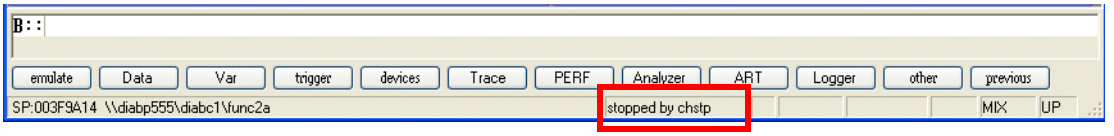
Format: **TrOnchip.Set** <*item*> **[OFF | ON]**

<*item*>: **CHSTPE ... SEIE** (only MPC500/800)

The program execution is stopped at the specified exception. For more details refer to the Debug Enable Register in your processor manual.

If program execution is stopped by an exception, the name of the exception is shown in the command line of TRACE32. Refer to the description of the Exception Cause Register in your processor manual for details.



TrOnchip.TCOMPRESS Trace data compression

Format: **TrOnchip.TCOMPRESS [ON | OFF]**

Not implemented yet.

TrOnchip.TEnable Set filter for the trace

Format: **TrOnchip.TEnable** <*par*>

Obsolete command. Refer to the **Break.Set** command to set trace filters.

TrOnchip.TOFF Switch the sampling to the trace to OFF

Format: **TrOnchip.TOFF**

Obsolete command. Refer to the **Break.Set** command to set trace filters.

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Format: **TrOnchip.TON EXT | Break**

Obsolete command. Refer to the **Break.Set** command to set trace filters.

TrOnchip.TTrigger Set a trigger for the trace

Format: **TrOnchip.TTrigger** <*par*>

Obsolete command. Refer to the **Break.Set** command to set a trigger for the trace.

TrOnchip.VarCONVert Adjust HLL breakpoint in on-chip resource

Format: **TrOnchip.VarCONVert [ON | OFF]**

Command is of no relevance for the MPC5xx/8xx family.

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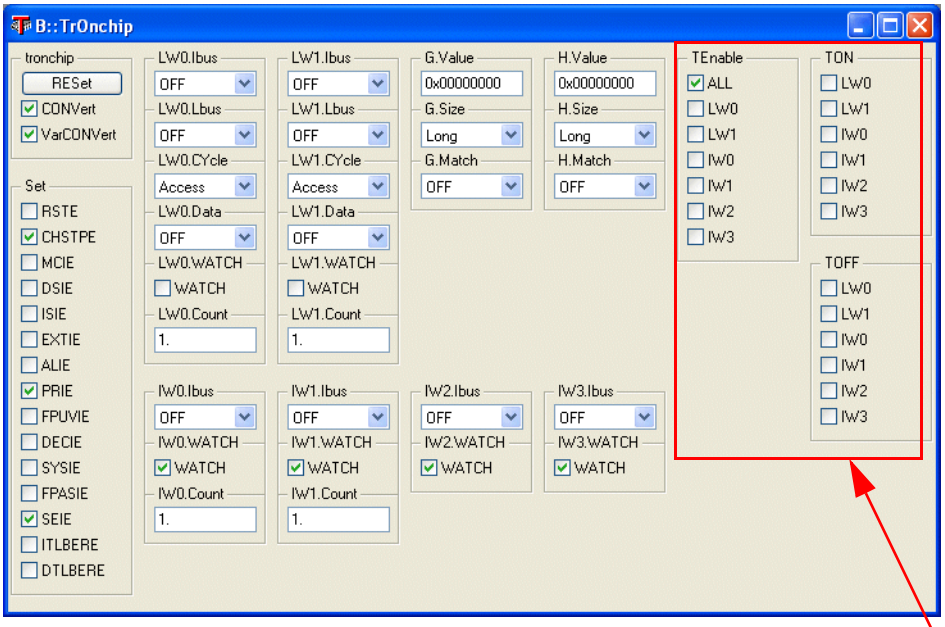
Format: **TrOnchip.view**

Display the TrOnchip window.



Only available if Preprocessor for MPC500/800 is used

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For information about *architecture-independent* **BMC** commands, refer to **"BMC"** (general_ref_b.pdf).

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10 pin BDM Connector MPC500/MPC800

Signal	Pin	Pin	Signal
VFLS0\FREEZE	1	2	SRESET-\RESETIN-
GND	3	4	DSCK
GND	5	6	VFLS1\FREEZE
RESETOUT-\HRESET-	7	8	DSDI
VDD	9	10	DSDO

The two signal names on pin 1. 2 and 6 have the same physical meaning. Only the use of the names differs between MPC500 and MPC800.

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Available Tools

CPU	ICE	FIRE	ICD DEBUG	ICD MONITOR	ICD TRACE	POWER INTEGRATOR	INSTRUCTION SIMULATOR
MGT560			YES		YES		YES
MPC533			YES		YES		YES
MPC534			YES		YES		YES
MPC535			YES		YES		YES
MPC536			YES		YES		YES
MPC555			YES		YES		YES
MPC556			YES		YES		YES
MPC561			YES		YES		YES
MPC562			YES		YES		YES
MPC563			YES		YES		YES
MPC564			YES		YES		YES
MPC565			YES		YES		YES
MPC566			YES		YES		YES
MPC821		YES	YES		YES		YES
MPC823		YES	YES		YES		YES
MPC850		YES	YES		YES		YES
MPC852T			YES		YES		YES
MPC855		YES	YES		YES		YES
MPC859DSL			YES		YES		YES
MPC859T			YES		YES		YES
MPC860		YES	YES		YES		YES
MPC862		YES	YES		YES		YES
MPC866P			YES		YES		YES
MPC866T			YES		YES		YES
MPC870			YES		YES		YES
MPC875			YES		YES		YES
MPC880			YES		YES		YES
MPC885			YES		YES		YES

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Language	Compiler	Company	Option	Comment
ADA	GNAT	Free Software Foundation, Inc.	ELF/DWARF	
C	CXPPC	Cosmic Software	ELF/DWARF	
C	CC	Freescale Semiconductor, Inc.	XCOFF	
C	XCC-V	GAIO Technology Co., Ltd.	SAUF	
C	GREEN-HILLS-C	Greenhills Software Inc.	ELF/DWARF	
C	GCC	HighTec EDV-Systeme GmbH	ELF/DWARF	
C	MCCPPC	Mentor Graphics Corporation	ELF/DWARF	
C	ULTRA-C	Radisys Inc.	ROF	
C	HIGH-C	Synopsys, Inc	ELF/DWARF	
C	DCPPC	TASKING	ELF/DWARF	
C	D-CC	Wind River Systems	IEEE	
C	D-CC	Wind River Systems	COFF	
C	D-CC	Wind River Systems	ELF/DWARF	
C++	GCC	Free Software Foundation, Inc.	ELF/DWARF	
C++	GREEN-HILLS-C++	Greenhills Software Inc.	ELF/DWARF	
C++	CCCPPC	Mentor Graphics Corporation	ELF/DWARF	
C++	MSVC	Microsoft Corporation	EXE/CV5	WindowsCE
C++	HIGH-C++	Synopsys, Inc	ELF/DWARF	
C++	D-C++	Wind River Systems	ELF/DWARF	
C++	GCCPPC	Wind River Systems	ELF/STABS	
C/C++	CODEWARRIOR	Freescale Semiconductor, Inc.	ELF/DWARF	
GCC	GCC	Free Software Foundation, Inc.	ELF/DWARF	
JAVA	FASTJ	Wind River Systems	ELF/DWARF	

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Name	Company	Comment
AMX	KadakProducts Ltd.	
ChorusOS	Oracle Corporation	
CMX-RTX	CMX Systems Inc.	
DEOS	DDC-I, Inc.	implemented by DDC-I
ECOS	eCosCentric Limited	1.3, 2.0 and 3.0
Elektrobit tresos	Elektrobit Automotive GmbH	via ORTI
ERCOSEK	ETAS GmbH	via ORTI
Erika	Evidence	via ORTI
FreeRTOS	Freeware I	v7
Linux	-	Kernel Version 2.4 and 2.6, 3.x, 4.x
Linux	MontaVista Software, LLC	3.0, 3.1, 4.0, 5.0
LynxOS	LynuxWorks Inc.	3.1.0, 3.1.0a, 4.0
MQX	Freescale Semiconductor, Inc.	3.x and 4.x
MQX	Synopsys, Inc	2.40 and 2.50
NetBSD	-	
NORTi	MISPO Co. Ltd.	
Nucleus PLUS	Mentor Graphics Corporation	
OS-9	Radisys Inc.	
OSE Delta	Enea OSE Systems	4.x and 5.x
OSEK	-	via ORTI
OSEKturbo	Freescale Semiconductor, Inc.	via ORTI/former MetrowerksOSEK
PikeOS	Sysgo AG	
ProOSEK	Elektrobit Automotive GmbH	via ORTI
pSOS+	Wind River Systems	2.1 to 2.5, 3.0, with TRACE32
QNX	QNX Software Systems	6.0 to 6.5.0
RTEMS	RTEMS	4.10
RTXC 3.2	Quadros Systems Inc.	
RTXC Quadros	Quadros Systems Inc.	
Sciopta	Sciopta	
SMX	Micro Digital Inc.	3.4 to 4.0
ThreadX	Express Logic Inc.	3.0, 4.0, 5.0
uC/OS-II	Micrium Inc.	2.0 to 2.92
uITRON	-	HI7000, RX4000, NORTi,PrKernel
VRTXsa	Mentor Graphics Corporation	
VxWorks	Wind River Systems	5.x to 7.x

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CPU	Tool	Company	Host
ALL	ADENEO	Adeneo Embedded	
ALL	X-TOOLS / X32	blue river software GmbH	Windows
ALL	CODEWRIGHT	Borland Software Corporation	Windows
ALL	CODE CONFIDENCE TOOLS	Code Confidence Ltd	Windows
ALL	CODE CONFIDENCE TOOLS	Code Confidence Ltd	Linux
ALL	EASYCODE	EASYCODE GmbH	Windows
ALL	ECLIPSE	Eclipse Foundation, Inc	Windows
ALL	RHAPSODY IN MICROC	IBM Corp.	Windows
ALL	RHAPSODY IN C++	IBM Corp.	Windows
ALL	CHRONVIEW	Inchron GmbH	Windows
ALL	LDRA TOOL SUITE	LDRA Technology, Inc.	Windows
ALL	UML DEBUGGER	LieberLieber Software GmbH	Windows
ALL	ATTOL TOOLS	MicroMax Inc.	Windows
ALL	VISUAL BASIC INTERFACE	Microsoft Corporation	Windows
ALL	LABVIEW	NATIONAL INSTRUMENTS Corporation	Windows
ALL	CODE::BLOCKS	Open Source	-
ALL	C++TEST	Parasoft	Windows
ALL	RAPITIME	Rapita Systems Ltd.	Windows
ALL	DA-C	RistanCASE	Windows
ALL	TRACEANALYZER	Symtavision GmbH	Windows
ALL	SIMULINK	The MathWorks Inc.	Windows
ALL	TA INSPECTOR	Timing Architects GmbH	Windows
ALL	UNDODB	Undo Software	Linux
ALL	VECTORCAST	Vector Software	Windows
ALL	WINDOWS CE PLATF. BUILDER	Windows	Windows
POWERPC	GR228X IC-TESTSYSTEME	Battefeld GmbH	Windows
POWERPC	OSE ILLUMINATOR	Enea OSE Systems	Windows
POWERPC	DIAB RTA SUITE	Wind River Systems	Windows

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Products

Product Information

OrderNo Code	Text
LA-7722 BDM-MPC500/800	**BDM Debugger for MPC500/800 (ICD)** supports PowerPC MPC505, MPC555, MPC56X MPC801, MPC821, MPC85x, MPC86x, MPC87x and MPC88x includes software for Windows, Linux and MacOSX requires Power Debug Module (Processor BDM input signals have to be 3.3V tolerant)

Order Information

Order No.	Code	Text
LA-7722	**BDM-MPC500/800**	**BDM Debugger for MPC500/800 (ICD)**

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